REMARKS

Present Status of the Application

Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement and the enable requirement. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton et al. (US 6,046,709A, hereinafter "Shelton") in view of Koyama et al. (US 2002/0021274 A1, hereinafter "Koyama"). Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton in view of Koyama and White et al. (US 7,634,668B2, hereinafter "White"). Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton, Koyama, and White as applied to claim 17 above, and further in view of Sheaffer et al. (US 6,593,930B1, hereinafter "Sheaffer").

In response thereto, Applicants have amended claims 1, 17, and 18 to overcome the rejections. Reconsideration and allowance of the application and presently pending claims 1-4 and 17-18 are respectfully requested.

Discussion for Claim Amendment

Applicants have amended claims 1, 17, and 18.

The features "the plurality of the blank periods of the display devices are in different frequencies" and "the least common multiple occurrences is a period that the blank periods of all display devices occur at the same time" are added into claims 1 and 17.

The features "the plurality of the blank periods of the display devices are in different frequencies" and "the least common multiple occurrences is a period that the blank periods of all display devices occur at the same time" are described and supported by Fig. 5 and related description of the present application. In Fig. 5, the blank period of the blank signal of the display devices DD1-DD3 are in the different frequencies, and the least common multiple occurrence is a period that the blank periods of all display devices DD1-DD3 occur at the same time(i.e. the period that the power saving process takes place). Therefore, based upon the interpretation above, it is believed that no new matter is added in amended claims 1 and 17.

Regarding claim 18, the features "while executing the power saving process, the system memory is continuously accessed by the CPU during the non-responding period of the CPU" is amended to "while executing the power saving process, the system memory is ~~continuously~~ accessed by the CPU during the non-responding period of the CPU". The amendments are supported by paragraph [0012] of the present application, which recites "[T]he present invention provides four different image data display mechanisms for continuously displaying image data/graphics data on multiple display devices computer system that contains a system memory directly accessed by the computer's CPU during the non-responding period of the CPU". Since the system memory is directly accessed by the computer's CPU during the non-responding

period of the CPU in the present application, the features "while executing the power saving process, the system memory is accessed by the CPU during the non-responding period of the CPU" can be supported thereby. Therefore, based upon the interpretation above, it is believed that no new matter is added in amended claim 18.

Discussion for 35 U.S.C. 103 Rejections to Claims

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton in view of Koyama.

Regarding claim 1, claim 1 is now recited as:

"A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside the CPU, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and synchronizing a plurality of blank periods of the display devices according to the common clock source, **the plurality of blank periods of the display devices are in different frequencies**;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process by the CPU during a non-responding period of the CPU, so as to reduce ~~a~~ consumptive power of the CPU, wherein memory access from the graphics-processing unit to the system memory through memory controller is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices, the least common multiple occurrence is a period that the blank periods of all display devices occur at the

same time." **(Emphasis Added)**

Shelton at least fails to disclose "**the plurality of blank periods of the display devices are in different frequencies**" and "**executing the power saving process within a least common multiple occurrence of the blank periods of the display devices, the least common multiple occurrence is a period that the blank periods of all display devices occur at the same time**". As admitted by Examiner, Shelton teaches "Such coordination is achieved by synchronizing the graphics boards 120 through an initialization process that sets all boards to **the same horizontal and vertical refresh frequencies**, and...". Though Shelton discloses the system frame display rate is set to be no greater than the slower of the two production rates, the vertical blank periods of monitors are set to substantially identical. That means, **although the frame production rates of graphics engines may differ, the display frequencies of the monitors are still the same**. However, **the present invention claims "the plurality of blank periods of the display devices are in different frequencies," not the frame production rate of graphics engine.**

Second, Shelton discloses comparing the frame production rates of two graphics engines, not the least common multiple occurrence of the vertical blank periods. As now amended in claim 1, the least multiple occurrence is the period that the blank periods of all display devices occur at the same time, as suggested in Fig. 5 of the present invention. The issue that Shelton concerns is to set the system frame display rate slower than all graphics engines so that all the display monitors may switch to a new frame at the same time. **Also as admitted by Examiner, Shelton fails to teach "executing the power saving process within a least common multiple occurrence of the blank periods of the display devices."**

Koyama fails to cure above deficiencies. First of all, Koyama does not deal with multiple display devices, thus nowhere throughout the description of Koyama does it discloses "providing a common clock source to the display devices and synchronizing a plurality of blank periods of the display devices, **the plurality of blank periods of the display devices are in different frequencies**."

Second, Koyama does not teach "executing the power saving process within a least common multiple occurrence of the blank periods of the display devices, the least common multiple occurrence is a period that the blank periods of all display devices occur at the same time.". Examiner tried to interpret the still image duration as the claimed least common multiple occurrence. However, as now amended, **the least common multiple occurrence is the period that the blank periods of all display devices occur at the same time**. As mentioned that **Koyama only deal with power saving of a single monitor, but the amended claim requires multiple display devices**.

Though Koyama teaches power saving process, but in combination with Shelton still fails to teach all limitations of the claims, especially "providing a common clock source to the display devices and synchronizing a plurality of blank periods of the display devices according to the common clock source, the plurality of blank periods of the display devices are in different frequencies" and "executing the power saving process within a least common multiple occurrence of the blank periods of the display devices, the least common multiple occurrence is a period that the blank periods of all display devices occur at the same time.". Accordingly, Applicants submit claim 1 should be patentable.

Claims 2-4 depend on claim 1. Since claim 1 is patentable, claims 2-4 are also patentable as matter of law.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton in view of Koyama and White.

The reasons of the patentability of claim 17 are same as those of claim 1, and therefore claim 17 should be patentable.

Claims 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton, Koyama, and White as applied to claim 17 above, and further in view of Sheaffer.

Claim 18 depends on claim 17. Since claim 17 is patentable, claim 18 is also patentable as matter of law.

To sum up, allowance of claims 1-4 and 17-18 is earnestly requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4 and 17-18 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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